AADL standards meeting Jan 25-27 2016

* Location Toulouse France. IRIT University.
  + Google map link - <http://maps.google.com/maps?q=Rue+Charles+Camichel,+31000+Toulouse,+France&z=16>
  + Address: IRIT/ENSEEIHT, 2 rue Charles CAMICHEL, 31071 TOULOUSE, FRANCE
  + Room location: Building E+F, room F501 (fifth layer, 2nd lift right in the hall of the building).
* Not collocated with ERTS2014 - <http://www.erts2014.org/>
* Information on hotels <https://wiki.sei.cmu.edu/aadl/index.php/AADL_meetings>

# Monday, Jan 25

* 0900-0945: AADL standardization committee news + action items (Bruce Lewis)
* 0945-1030: AADL v3 roadmap review (Peter Feiler)
* 1030-1100: break
* 1100-1230: AADL v3 discussions (Nested processors, virtual memory & memory configurations) (Peter Feiler)
* 1230-1400: Lunch
* 1400-1530: AADL v3 discussions (Configuration & Binding) (Peter Feiler)
* 1530-1600: Break
* 1600-1730: AADL v3 discussions (Compositional Interfaces) (Peter Feiler)
* 1730-1815: Update on the IRT Rover Project (Patrick Farail, Pierre Gaufillet, Jerome Hugues)

# Tuesday, Jan 26

* 0900-1030: AADL v3 discussions (array connections, unified type systems)
* 1030-1100: break
* 1100-1230: AADL Core Errata (Peter Feiler)
* 1230-1400: Lunch
* 1400-1530: AADL BA Errata (Etienne Borde)
* 1530-1600: Break
* 1600-1800: AADL BA Update (Etienne Borde, Jean-Pierre Talpin, Brian Larson)

# Wednesday, Jan 27

* 0900-1000: Network Annex Update (Alexey Khoroshilov, Tiyam Robati, Brendan Hall)
* 1000-1030: Expression language and Constraints Annex Draft plus Update (Serban Gheorghe)
* 1030-1100: break
* 1100-1230: Expression Language and Constraint Annex Update (Serban Gheorghe)
* 1230-1400: Lunch
* 1400-1500: Remaining issues BA, Constraints, or V3
* 1500-1530: Plan next meeting
* 1530-1600: Break
* 1600-1800: D-MILS and MILS-AADL (Thomas Noll)

Webex Info: